

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: INTEGRATED INDUCTIVE CIRCUITS

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Express Mail No.: EL857974068US

Date: February 21, 2002

2002-02-21 14:00:00

INTEGRATED INDUCTIVE CIRCUITSBackground

This invention relates generally to radio frequency (RF) integrated circuits that include active devices and passive components such as inductors and capacitors used for radio frequency devices such as cellular telephones and wireless network devices such as Bluetooth and other wireless devices and personal digital assistants.

The technology for manufacturing integrated circuits has conventionally divided integrated circuits into various categories based on the compatibility of processes and other considerations. Generally, radio frequency circuits have not been mixed with logic circuits in the same integrated circuit. Radio frequency circuits are analog circuits that are involved in filtering and detecting radio frequency signals such as cellular telephone signals. In contrast, logic circuits generally include transistors and other active components that form digital integrated circuit devices. Thus, for example, bipolar techniques may be utilized to manufacture radio frequency circuits and standard complementary metal oxide semiconductor (CMOS) processes may be utilized to manufacture logic circuits.

Memory circuits may account for still another category. Generally, special processes may be utilized in

connection with the manufacture of memory circuits because of special design considerations such as multiple gate electrodes and special voltage supply needs. Thus, memory circuits are often fabricated separately from logic circuits.

Still another category are the so-called mixed signal circuits which may include both digital and analog components. These signals too may be accounted for separately so that a device that includes RF signal processing, RF integrated circuits, mixed signal circuits, logic circuits and memory circuits may be made up of a number of separately fabricated integrated circuit chips.

The cost of an electronic device may be closely correlated to the extent of integration that is possible. The more devices and the more types of devices that can be integrated into a single integrated circuit and manufactured using highly replicated techniques, the lower the resulting price. Unfortunately, because of incompatibilities between the different types of integrated circuits, it has not been possible, to date, to fabricate both radio frequency circuits, mixed signal circuits, logic circuits and memory circuits all on the same standard CMOS integrated circuit process.

One problem that arises in connection with radio frequency circuits in CMOS processes is that the passive components such as capacitors and inductors may be

adversely affected by the substrates over which they are formed. In particular, coupling may occur between the substrate and integrated circuit inductors for example. This coupling may result in degraded performance of inductive circuits. As a result, inductive circuits may be formed in bipolar or silicon over insulator (SOI) integrated circuits rather than using standard CMOS logic processes. Thus, two or more integrated circuits are needed--one for logic, one for RF circuits, one for memory and one for mixed signals.

Some efforts have been made to overcome this coupling problem. For example, Silicon Wave Inc. has devised a so-called silicon over insulator (SOI) BiCMOS (Bipolar CMOS) integrated circuit which integrates both logic and radio frequency components onto the same die. However, the use of silicon over insulator technology greatly complicates the manufacturing process and increases cost. Moreover, the bulk of semiconductor fabrication facilities in the United States and the rest of the world are dedicated to manufacturing metal oxide semiconductor technologies. The SOI process is not amenable to widespread manufacturing at a number of highly expensive, already existent, fabrication facilities.

In addition to capacitive coupling of substrate noise, magnetic coupling between integrated inductors on the same integrated circuit may also be problematic. The coupling

between integrated inductors on the same circuit may adversely effect the operation of any given inductor. For example, the magnetic coupling may change the operating parameters of one or more integrated inductors on the same integrated circuit.

The quality factor or Q factor strongly depends on the layout and the properties of the particular process technology. It is known that the quality of an integrated inductor may be adversely affected by the metal wire resistance, capacitive coupling to the substrate and magnetic coupling to the substrate. Capacitive and magnetic coupling limit the Q factor at relatively high frequencies. The magnetic coupling becomes more significant in CMOS technologies with doped substrates because the effect of substrate resistance appears in parallel with the inductor.

Thus, there is a substantial need to find a way to reduce coupling in integrated inductors.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of one embodiment of the present invention;

Figure 2 is an enlarged cross-sectional view of one stage in the sequence of making the device shown in Figure 1 in accordance with one embodiment of the present invention; and

Figure 3 is an enlarged cross-sectional view of another stage in the sequence of manufacturing the device shown in Figure 1 in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, an integrated inductor 20 may be formed over a field oxide region 18 in turn formed over a semiconductor substrate 12. This substrate 12 has an aperture 14 formed therein that is filled with a dielectric material 16. In one embodiment, the aperture 14 may be a conical section.

Referring to Figure 2, the sequence of making the device shown in Figure 1 may begin by forming a field oxide region 18 over a substrate 12. The integrated inductor 20 is then patterned on top of the field oxide region 18. A variety of techniques may be utilized for forming integrated inductor 20. Commonly the integrated inductor 20 may have a spiral configuration. However, any of a variety of integrated inductors may be utilized in embodiments of the present invention.

The integrated inductor 20, if formed in the fashion shown in Figure 2, may experience capacitive and magnetic coupling with other components formed in the same substrate 12. It may be desirable to form the inductor 20 together with other components in the same substrate 12. Those other components may include a variety of other devices

including logic, memory, and mixed signal devices.
Particularly, where the inductor 20 is utilized in a radio
frequency circuit, the capacitive and magnetic coupling
through the substrate 12 may become problematic especially
5 at relatively high frequencies.

In order to address these concerns, in accordance with
one embodiment of the present invention, an aperture 14 may
be etched from the back side 22 of the substrate 12 to form
an aperture 14 as shown in Figure 3. The etching process
10 used to form the aperture 14 may be any conventional
anisotropic or isotropic back side etch. In one
embodiment, the etching may extend completely through the
substrate 12 to the field oxide region 18. Thus, an
etching process may be utilized that uses the field oxide
15 region 18 as an etch stop in one embodiment.

As a result of the back side etch used to form the
aperture 14, a floating membrane inductor 20 may be formed
in one embodiment. Thereafter, the aperture 14 is filled
with a dielectric material 16, as shown in Figure 1. The
20 dielectric material 16 may be deposited, spun-on or applied
by any other technique. Any of a variety of dielectric
materials are suitable. In one embodiment, the dielectric
material 16 is coated over the backside 22 of the substrate
12 as indicated at 16a.

25 After the die is completed with the dielectric
material 16 in place, a conductive or nonconductive epoxy

may be utilized to attach the die to a leadframe (not shown) of a semiconductor package. The epoxy will not degrade the inductor's performance because of the presence of the dielectric layer 16, including in some embodiments the portion 16a completely covering the back side 22 of the substrate 12, as shown in Figure 1. In addition, the dielectric material 16 may provide structural support in the region of the substrate 12 where the aperture 14 was formed.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: